Amendments to the Claims:

14. (NEW) An asymmetric static random access memory (SRAM) cell operable with a supply voltage to store a one or a zero, the asymmetric SRAM cell further comprising:

at least two cross-coupled inverters, one having an output electrically connected to a bit line bar when a word line is held high and the other having an output electrically connected to a bit line when a word line is held high and further comprising a pull-down transistor; and

a pass transistor connected to a gate of the pull-down transistor so that a voltage across the gate is reduced relative to the supply voltage, thereby reducing leakage through the gate when the asymmetric SRAM cell is storing a zero.

15. (NEW) The asymmetric SRAM cell of claim 14 wherein a voltage at a gate of the pass transistor is reduced relative to the supply voltage to further reduce leakage through the gate of the pull-down transistor.

16. (NEW) The asymmetric SRAM cell of claim 14 wherein the first and second inverters comprise a plurality of transistors further comprising at least one first type of transistor and at least one second type of transistor that is weaker than the first type of transistor.

17. (NEW) The asymmetric SRAM cell of claim 16 interconnected with a plurality of like SRAM cells and a sense amplifier further comprising pairs of cross-coupled inverters and a plurality of sense amplifier transistors forming a dummy column of cells.